REMARKS

Claims 34 and 36-46 are now in the application and are directed to the elected species. Independent claim 42 combines the features from prior claims 32 and 33 as well as clarifying that the circuit lines with the second top surface of the second dielectric layer of polymeric material.

Claims 32, 34 and 35 were rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,274,821 to Echigo et al. This rejection of the claims has been rendered moot by newly presented claim 42 which recites the presence of a seed layer as recited in prior claim 33. Claim 33 was not rejected on the above ground.

Claims 33, 37, 40 and 41 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,274,821 to Echigo et al. in view of U.S. Patent 6,323,435 to Strandberg et al. The cited references do not render obvious the present invention.

The present invention provides for obtaining a structure having embedded flush circuitry features. The present invention makes it possible to create circuitry features that are much more densely configured than those fabricated using current methods. This is made possible since the final structure is a circuitry feature having dielectric regions and conductive features that are coplanar.

In particular, the present invention relates to a structure comprising a first dielectric layer of a polymeric material having a first top surface; a second dielectric layer of a polymeric material on the first top surface of the first dielectric layer of a polymeric material, having a second top surface, the second layer of polymeric material also having trench features therein; seed layer located in the trenches; electrically conductive material deposited in the trench features forming electrically conductive circuit lines and being substantially flush with the second top surface of the second dielectric layer of polymeric material.

Moreover, the structure of claim 42 and claims dependent thereon include a third dielectric layer of polymeric material located on the electrically conductive circuit lines.

The present invention is especially advantageous for fabricating buried interconnection levels that are in close proximity to one another in a printed circuit board structure.

As discussed in the specification, printed circuit board interconnection levels prior to the present invention are built on top of a dielectric thin film layer. Circuitry features are formed using photolithographic and subtractive etch techniques. In a typical method, a metallic foil and especially copper foil is laminated to the substrate followed by using photolithographic and subtractive etching to create the circuitry. The copper foil includes a roughened or dendritic backside surface for inducing mechanical adhesion to the substrate. Smooth copper layers do not adequately bond without and auxiliary bonding agent.

Great difficulties exist in adequately etching dendrites especially when dealing with small spaces. Moreover, along with the concern created by dendrites, the width of the lines (e.g. about 0.5 mils wide), and photolithographic issues (e.g. resolution of fine features, 0.7 mil wire with 1/1 mil space, in a thin photo resist film), and subtractive etch undercut/pad rounding, render clearly and fully resolving small line spaces such as the 1.8 mil pitch features presently desired very difficult. Additionally, this subtractive etch approach results in unprotected circuitry features referred to as "skyscrapers" that extend above an underlying plane of dielectric barrier material.

In many structures, it is important to plate another metal such as gold or nickel-gold onto the copper circuitry. The "skyscraper" structure causes a problem of bridging or shorting between lines especially where there exist closely spaced fingers.

As discussed in the specification, the present invention addresses these concerns of the prior art.

U.S. Patent 6,274,821 to Enchigo et al. fails to render obvious the present invention since, among other things, Echigo does not suggest a structure being a first dielectric layer of polymeric material and a second dielectric layer of polymeric material on top of the first dielectric layer and trenches in the second dielectric layer. Furthermore, it is not apparent wherein Echigo et al. suggests circuit lines that are formed in the trenches and are substantially flush with the top surface of a second dielectric layer.

On the other hand, Echigo et al. describes a structure which starts with an initial dielectric layer that has holes drilled and metallized by plating or Cu paste. This is in contrast, as discussed above, with the present invention which starts out with an initial dielectric structure followed by a second before metallization occurs. Moreover, Echigo et al. does not even describe any method for patterning and metallization, but merely refers to an initial dielectric substrate with metallized holes.

U.S. Patent 6,323,435 does not overcome the above discussed deficiencies of Echigo et al. with respect to rendering obvious the present invention. Strandberg was relied upon for a disclosure of a seed layer for forming the conductive patterns on a dielectric material. U.S. Patent 6,323, 435 merely describes a method of embedding circuits by adding sequential layers of dielectric. It also starts with a base substrate of dielectric with "raised" conductor features already in place. It creates the look of flushness by the subsequent applications of dielectric layers over the base conductors. This is quite different from the structure of the present invention having circuit lines in trenches in a second direction and being flush with the top surface of the second dielectric.

Claims 36, 38 and 39 were rejected under 35 U.S.C 103(a) as being unpatentable over U.S. Patent 6,274,821 to Echigo et al. in view of U.S. Patent 6,586,682 to Strandberg et al. U.S. Patent 6,586,682 to Strandberg et al. does not overcome the above discussed deficiencies of Echigo et al. with respect to rendering obvious the present

invention. Strandberg et al. was relied upon for a disclosure of thicknesses as recited in claims 36, 38 and 39.

Contrary to the present invention, U.S. Patent 6,586,682 to Strandberg et al. describes a planarization process by adding 2 dielectric layers to an already personalized dielectric substrate with "raised" conductor pattern.

In view of the above, consideration and allowance are, therefore, respectfully solicited.

In the event that the Examiner believes an interview might serve to advance the prosecution of this application in any way, the undersigned attorney is available at the telephone number noted below.

The Commissioner is hereby authorized to charge any fees or credit any overpayment associated with this communication including any extension fees to Deposit Account No. 22-0185.

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Respectfully submitted,

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